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LIST OF PRIOR ART CITED BY APPLICANT				APPLICANT(S) KyeHyung LEE et al.				
(PTO-1449)				FILING DATE December 31, 2003		GROUP 28/6		
U.S. PATEN	T DOCUMENTS	<u> </u>		· · · · · · · · · · · · · · · · · · ·			· · ·	
EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME		CLASS	SUBCLASS		ING
lny	6,351,191	02/26/02	Nair et al.		331	57		
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EXAMINER'S	AND LOSS ASSESSED OF	Marining Marine	DREIGN RATENT	DOCUMENTS: 🛧				
INITIALS	PATENT NO.	PATENT NO. DATE		OUNTRY	CLASS	SUBCLASS	Transi Yes	No No

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OTHER A	ART (Including A	Author, Title,	Date, Pertine	nt Pages, Publis	her, Place o	of Publication	ı, Etc.)	
	Noda et al. "AN ON-CHIP TIMING ADJUSTER WITH SUB-100-PS RESOLUTION FOR A HIGH-							
LAN	SPEED DRAM INTERFACE," 1998 Symposium on VLSI Circuits Digest of Technical Papers, pages 62-63							
<u> </u>	pages of to							
	John G. Maneatis "LOW-JITTER PROCESS-INDEPENDENT DLL AND PLL BASED ON SELF-							
Ind	BIASED TECHNIQUES," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996.							
	pages 1723-1732							
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